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(54) Name of Invention: Method of Fabricating Semiconductor Device

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Specifications

1. **Name of Invention:** Method of Fabricating Semiconductor Device

2. **Scope of Patent Application:** A method of fabricating semiconductor devices which is characterized by using a process that forms thin organic silicon films on semiconductor substrates, and a process that removes the thin organic silicon film's organic functional group from the surface to a prescribed depth so as to form a dual-layered structure of silicon oxide film and thin organic silicon film on the semiconductor substrate.

3. **Detailed Explanation of Invention**

Field for Commercial Utilization: This invention relates to a method for fabricating highly reliable semiconductor devices having a multilayer wiring structure.

Existing Technology: In order to get highly reliable multilayer wiring structures in semiconductor devices it is necessary to flatten the films between the metallic wiring layers. For the usual flattening, etch-back methods and lift-off methods are used. These methods are premised on interlayer films completely embedding the spaces between the metallic wiring. However, in recent years, with the high integration of semiconductor devices, these spaces between metallic wiring have become small, making it difficult to embed dielectric films. So, it has become difficult to do the flattening by the above methods.

Of late, a bias-sputter method has been found that can embed dielectric film even in narrow spaces between the metallic wiring; but bias sputtering has the shortcoming of damaging elements formed on the substrate. So, what has been drawing attention is a method called spin-on glass. In this, a solution containing organic or inorganic silicon is applied to the substrate and heat is applied to form a thin organic or inorganic film to make it possible to embed and flatten even narrow spaces between the metallic wiring by forming dielectric film with liquid applications. Yet, the spin-on glass method has a defect: cracks or peeling easily occurring in the silicon oxide film that the spin-on glass method creates, meaning that insulating properties of thin organic silicon films formed this way are inadequate.

Problems the Invention Seeks to Resolve: To get semiconductor devices with a highly reliable multilayered wiring structure, the film between metallic wiring layers must be flattened. But, as discussed above, now with the advance in element miniaturization, present methods of flattening have reached their limit. So, we inventors have considered the shortcomings in the existing methods and looked into a spin-on glass method that could cope, even as miniaturiz-ation of elements proceeds. Thus, we came to complete this invention as a result of studies and research on methods that would do flattening by using the spin-on glass method but combine the strengths of both silicon oxide film and thin organic silicon film with a method that would not generate cracks or flaking off even when the insulativity is made high.

Means to Resolve Problems: Change to a dual-layer structure--a silicon oxide film layer and a thin organic

silicon film layer--by applying a solution containing organic silicon to a semiconductor substrate having an irregular surface, doing heat processing and then exposing the substrate to an oxygen plasma to remove the thin organic silicon film surface's organic functional group.

Effects: When, after making the thin organic silicon film, one exposes it to an oxygen plasma to create a dual-layered structure of silicon oxide film and thin organic silicon film, the presence of thin organic silicon film below makes it difficult for cracking or peeling to occur. Also, since it is silicon oxide film that is in contact with the overlying metallic wiring, the insulating properties are sufficient. Semiconductor devices are thus yielded that have a multi-layered wiring structure of high reliability.

Application Example: Below, we will explain this invention in detail, based on the figures.

Figures 1 to 4 are enlarged partial cross sections showing the processes of one application example of a semiconductor device from this invention.

In Figure 1, after forming field oxide film 2 by using the selective oxidation method on semiconductor substrate 1, one successively forms gate oxide film 2 and polysilicon gate 4 and uses ion-injection to install dispersion layer 5 in the source/drain area. Next, one forms 1st interlayer dielectric film 6 of phosphor-boron glass or the like, and makes contact hole 7 by anisotropic etching. On top of this is formed 1-μ thick aluminum wiring 8 and then 2nd interlayer dielectric film 9 of about 5000Å. For 2nd interlayer dielectric film 9 a silicon oxide film or the like made by plasma CVD is suitable. Then one applies about 3000Å of a solution containing organic silicon. For this one uses a solution with a chemical having a structure of $(C_6H_5)_nSi(OH)_{4-n}$. As the liquid containing organic silicon is inserted into narrow grooves, irregularities present before the application can be mostly eliminated.

Next one does heat processing of semiconductor substrate 1 (raising the temperature in several stages from room temperature, ending at 450°C after 30 minutes) to form thin organic silicon film 10 (Fig. 2). After that, one exposes semiconductor substrate 1 to an oxygen plasma for 10 minutes to remove thin organic silicon film 10's organic functional group to a prescribed depth, converting it to a silicon oxide film. That makes most of the thin parts of the thin organic silicon film formed initially into silicon oxide

film so that only the thick film areas remain as thin organic silicon film 10 in a dual-layer structure with silicon oxide film 11 (Figure 3). Through hole 12 is opened between the wiring layers on the substrate and 2nd aluminum wiring 13 is formed (Fig. 4). Because the organic silicon liquid was applied onto the substrate to flatten it, 2nd aluminum wiring 13 will not easily get broken wires or shorts. Moreover, since it is silicon oxide film 11 that is in direct contact with 2nd aluminum wiring 13, the insulating traits are sufficient. Again, the thick places between 1st aluminum wiring 8 and 2nd aluminum wiring 13 have the dual-layer structure of silicon oxide film and thin organic silicon film and since the thin organic silicon film is the lower layer, cracks will not easily intrude.

It is desirable that the solution containing organic silicon used in this invention's fabricating method include compounds having the structure of $RnSi(OH)_{4-n}$ (R: alkyl base) or $Si(OR)_4$ (R: alkyl base). Of these the $(C_6H_5)_nSi(OH)_{4-n}$ solution used in this application example showed very superior properties.

Invention's Effectiveness: If one uses the fabricating method of this invention, one can flatten interlayer films between metallic wiring layers by simple processes. Also, since silicon oxide film and thin organic silicon film are combined, one can get semiconductor devices which have good insulativity, which scarcely gets cracks or peeling and whose reliability is high.

Because flattening is done by a liquid application, the fabricating method of this invention can cope even with further advances hereafter in element miniaturization. Such a fabrication method has a very high commercial value not seen elsewhere.

4. Simple Explanation of Figures

Figures 1 through 4 show the processes of one application example when fabricating a semiconductor device with this invention. Figure 1 is an enlarged partial cross section of a semiconductor device using the fabricating method from this invention. Figure 2 is an enlarged partial cross section of a semiconductor substrate after the thin organic silicon film is formed. Figure 3 is an enlarged partial cross section of a semiconductor substrate after exposure to

oxygen plasma. Figure 4 is an enlarged partial cross section after 2nd aluminum wiring is formed using the fabrication method of this invention.

1 … Semiconductor substrate
2 … Field oxide film
3 … Gate oxide film
4 … Polysilicon gate
5 … Dispersion layer
6 … 1st interlayer dielectric film
7 … Contact hole
8 … 1st aluminum wiring
9 … 2nd interlayer dielectric film
10 … Thin organic silicon film
11 … Silicon oxide film
12 … Through hole
13 … 2nd aluminum wiring

Agent's name: Toshio Nakao, Patent attorney (and one other)

TRANSLATION

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Japanese Published Examined Patent Application 63-157443, Published June 30, 1988; Application Filing No. 61-305736, Filed December 22, 1986; Inventor: Kiyoyuki MORITA; Assignee: MATSUSHITA ELECTRIC CORP.

MANUFACTURING METHOD FOR SEMICONDUCTOR DEVICE

[CLAIM]

A manufacturing method for a semiconductor device, characterized in comprising a step of forming an organic silicon thin film atop a semiconductor substrate, and a step of removing the organic functional groups of the organic silicon thin film from the surface to a desired depth so as to form a two-layer structure of a silicon oxide layer and an organic silicon thin film layer atop the semiconductor substrate.

[DETAILED DESCRIPTION OF THE INVENTION]

[PRIOR ART]

The present invention concerns methods for manufacturing semiconductor devices that have a highly reliable multi-layer wiring structure.

[PRIOR ART]

In order to obtain highly reliable multi-layer wiring structures in semiconductor devices, there is a necessity to planarize the intermediate film between metal wiring layers. Prior art planarization methods utilize etch-back and/or lift-off methods. These methods presuppose the total embedding of the intermediate film in the gap between wiring layers. However, in recent years, along with the increasing

integration of semiconductor devices, the gap between wiring layers has narrowed, such that it has become difficult to embed an insulating film into the gap thereof. As such, it is difficult to achieve planarization with said methods. In recent years, bias sputtering methods capable of embedding an insulation film even into narrow gaps between wiring layers have been developed, but bias sputtering methods have the disadvantage of causing damage to elements formed atop the substrate. As such, a method called a spin-on glass method has recently gained attention. This method involves the formation of an organic or inorganic thin-film by the addition of a coating and heat-treatment of an organic or inorganic silicon-containing solution atop a substrate, and because an insulating film is formed by the coating of the liquid, even narrow gaps between wiring layers can be embedded and planarized. However, there is a disadvantage that cracks and peeling are easily generated in the silicon oxide film formed by spin-on glass methods, and although cracks and peeling are not easily generated in the organic silicon thin film formed by spin-on glass methods, there is a disadvantage that the insulating characteristics thereof are inadequate.

[PROBLEM OF PRIOR ART TO BE ADDRESSED]

In order to obtain highly reliable multi-layer wiring structures in semiconductor devices, there is a necessity to planarize the intermediate film between metal wiring layers. However, as disclosed above, in the current state of affairs

wherein element miniaturization has been continuing, prior art planarization methods have come to reach their limits. As such, the present inventors observed the disadvantages of prior art method; paying attention to spin-on glass methods capable of corresponding to the miniaturization of elements, the result of their various research into methods wherein the advantages of both silicon oxide films and organic silicon thin films could be combined while obtaining high reliability and no generation of cracks or peeling while effecting planarization using said spin-on glass methods, was the completion of the present invention.

[MEASURES TO SOLVE THE PROBLEM]

A solution containing organic silicon is coated atop a semiconductor substrate that has an uneven surface; after applying a heat treatment, the substrate is exposed to an oxygen plasma such that organic functional groups of the surface of the organic silicon thin film are removed, and a two-layer structure of a silicon oxide film and an organic silicon thin film is obtained.

[FUNCTION]

After forming the organic silicon thin film, and obtaining a two-layer structure of a silicon oxide film and an organic silicon thin film by exposure to oxygen plasma, because an organic silicon thin film is present on the bottom unit, cracks, peeling, and the like do not easily occur. Furthermore, because the silicon oxide film is in contact with the metal wiring of the upper unit, insulating

characteristics are adequate. In this way, a semiconductor device having a highly reliable multi-layer wiring structure can be obtained.

[EMBODIMENT]

An embodiment of the present invention will be explained in detail hereinbelow based on the drawings.

Figures 1 through 4 are partial expanded cutaway views showing the steps of an embodiment of the manufacturing method for a semiconductor device of the present invention.

In figure 1, after forming field-oxide film 2 using a selective oxidation method atop semiconductor substrate 1, gate oxide film 3 and polysilicon gate 4 are formed in order, and by an ion implantation method a dispersion layer 5 is provided in the source and drain region. Next, a first inter-layer insulation film of boro-phosphate glass or the like is formed, and contact hole 7 is formed by anisotropic etching. A 1μ thick first aluminum wiring 8 is formed thereatop, and then a second insulating film is formed at a thickness of roughly 5,000 Angstroms. As for this second intermediate insulation film 9, a silicon oxide film formed by plasma CVD is appropriate. Next, a solution containing organic silicon is coated thereupon at roughly 3000 Angstroms. As for this solution containing organic silicon, a solution containing a compound having the structure $(C_6H_5)_nSi(OH)_{4-n}$ is used. Because the solution containing organic silicon infiltrates small groove units, it can nearly completely alleviate the unevenness that existed atop

the substrate prior to coating. Next, semiconductor substrate 1 is heat-treated (temperature is raised in stages from room temperature, to a final temperature of 450 degrees Celsius for 30 minutes) such that organic silicon thin film 10 is formed (figure 2). When this semiconductor substrate 1 is exposed to an oxygen plasma for ten minutes, the organic functional groups of organic silicon thin film 10 are removed to a desired depth, transforming into a silicon oxide film. As such, the film thickness of organic silicon thin film 10 as initially formed, in its thinnest portions, transforms nearly entirely to silicon oxide film 11; only in the thickest portions does it come so as to have a two-layer structure of silicon oxide film 11 and organic silicon thin film 10 (figure 3). Through-hole 12 of the intermediate wiring layer is provided atop the substrate, and second aluminum wiring 13 is formed (figure 4). Because coating of a solution containing organic silicon so as to effect planarization is undertaken atop the substrate, second aluminum wiring 13 does not easily generate short-circuits or cut wires. Furthermore, because silicon oxide film 11 is in direct contact with second aluminum wiring 13, the insulating characteristics are adequate. Furthermore, the thick portions of the intermediate film of first aluminum wiring 8 and second aluminum wiring 13 come to have a two-layer structure of silicon oxide film and organic silicon thin film, such that because an organic silicon thin film

layer is present on the bottom layer, it is difficult for cracks to infiltrate.

As for the organic silicon-containing solution used by the manufacturing method of the present invention, an article containing a compound having the structure $RnSi(OH)_{4-n}$ (wherein R = alkyl group) or $Si(OR)_4$ (wherein R = alkyl group) is preferable; among these, however, the solution containing $(C_6H_5)_nSi(OH)_{4-n}$ as used in the embodiment displays superior characteristics.

[EFFECT]

By using the manufacturing method as by the present invention, the intermediate film between the wiring layers can be planarized by a simple step. Furthermore, because a silicon oxide film and an organic silicon thin film are combined, a highly reliable semiconductor device with high insulation characteristics and wherein cracks and peeling are not easily generated can be obtained.

The manufacturing method as by the present invention effects planarization by coating with a liquid; because of this, it can be applied even in the face of future miniaturization of elements. This type of manufacturing method is totally novel, and has an extremely high utility value from an industrial standpoint.

[BRIEF DESCRIPTION OF THE DRAWINGS]

Figures 1 through 4 show an embodiment of manufacturing a semiconductor device by the present invention. Figure 1 is a partial expanded cutaway view of a semiconductor

substrate; figure 2 is a partial expanded cutaway view of a semiconductor substrate after forming of an organic silicon film; figure 3 is figure 2 is a partial expanded cutaway view of a semiconductor substrate after exposure to oxygen plasma; figure 4 figure 2 is a partial expanded cutaway view of a semiconductor substrate after formation of the second aluminum wiring layer.

1 - Semiconductor substrate; 2 - Field oxide film; 3 - Gate oxide film; 4 - polysilicon gate; 5 - Dispersion layer; 6 - First interlayer insulation film; 7 - Contact hole; 8 - First aluminum wiring; 9 - Second interlayer insulation film; 10 - Organic silicon thin film; 11 - Silicon oxide film; 12 - Through-hole; 13 - Second aluminum wiring

USPTO TRANSLATIONS BRANCH

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TITLE: MANUFACTURE OF SEMICONDUCTOR DEVICE

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ABSTRACT:
PURPOSE: To constitute a two-layer structure of a silicon oxide film layer and an organic silicon thin film layer, and obtain a semiconductor element with highly insulative property by a simple process, by a method wherein a substrate is exposed in oxygen plasma, and the organic functional group of an organic silicon thin film is removed, after a liquid containing organic silicon is spread on a semiconductor substrate having unevenness on the surface and a heat treatment is performed.

CONSTITUTION: After a field oxide film 2 is formed on a semiconductor substrate 1, a gate oxide film 3 and a polysilicon gate 4 are formed in order, and a diffusion layer 5 is formed in a source.drain region by an ion implantation method. After a first interlayer insulating film 6 is formed, contact holes 7 are formed by anisotropic etching. On the holes 7, an aluminum wiring with specified thickness is formed, and thereon, a second interlayer insulating film 9 with specified thickness is formed. A liquid containing organic silicon is spread, which is made an organic silicon thin film 10 by thermal treatment. Then the substrate 1 is exposed to oxygen plasma, and a two-layer structure of the thin film 10 and a silicon oxide film 11 is obtained.

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審査請求　未請求　発明の数 1　（全4頁）

㊹発明の名称　半導体装置の製造方法

㉑特　願　昭61－305736

㉒出　願　昭61(1986)12月22日

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明　細　書

1、発明の名称

半導体装置の製造方法

2、特許請求の範囲

半導体基板上に有機シリコン薄膜を形成する工程と、有機シリコン薄膜の有機官能基を表面から所定の深さまではずす工程により、半導体基板上にシリコン酸化膜層と有機シリコン薄膜層の2層構造を形成することを特徴とする半導体装置の製造方法。

3、発明の詳細な説明

産業上の利用分野

本発明は、信頼性の高い多層配線構造を持つ半導体装置を製造する方法に関する。

従来の技術

半導体装置において、信頼性の高い多層配線構造を得るためには、金属配線層間の層間膜を平坦化する必要がある。従来この平坦化には、エッチバック法やリフトオフ法が用いられてきた。これらの方法は層間膜が金属配線間のすきまを完全に埋めることが前提となっている。ところが近年、半導体装置の高集積化に伴い、金属配線間のすきまが狭くなり、そのすきまに絶縁膜を埋め込むことが困難になった。よって上記の方法では平坦化が難しい。近年、金属配線間の細いすきまにも絶縁膜を埋め込むことできるバイアススパッタ法が開発されたが、バイアススパッタ法には、基板上に形成された素子にダメージを与えるという欠点がある。そこで現在注目を浴びているのがスピンオングラス法と呼ばれる方法である。これは、無機または有機シリコン含有液を基板上に塗布し熱処理を加えて無機または有機シリコン薄膜を形成するものであり、液体の塗布で絶縁膜を形成するために金属配線間の細いすきまも埋めて平坦化することが可能となる。しかし、スピンオングラス法で形成したシリコン酸化膜にはクラックや剥離が生じやすいという欠点があり、スピンオングラス法で形成した有機シリコン薄膜には、クラックや剥離は生じにくいが絶縁特性が十分でないという欠点があった。

発明が解決しようとする問題点

信頼性の高い多層配線構造を有する半導体装置を得るためには、配線金属層間の層間膜を平坦化する必要がある。ところが前述の通り、素子の微細化が進んだ現在、従来の平坦化法では限界にきている。そこで本発明者は従来の方法の諸欠点を鑑み、今後さらに素子の微細化が進んでも対応の可能なスピンオングラス法に注目し、スピンオングラス法を用いて平坦化を行うとともに、シリコン酸化膜、有機シリコン薄膜両方の長所を組み合わせて、絶縁性が高くしかもクラックや剥離が生じない方法を種々考案研究した結果、本発明を完成するに至ったものである。

問題を解決するための手段

表面に凹凸を有する半導体基板上に有機シリコン含有液を塗布し、熱処理を加えた後基板を酸素プラズマ中にさらして有機シリコン薄膜表面の有機官能基をはずしシリコン酸化膜層と有機シリコン薄膜層の２層構造に変える。

作　用

有機シリコン薄膜を形成後、酸素プラズマにさらしてシリコン酸化膜層と有機シリコン薄膜層の２層構造にすると、下部に有機シリコン薄膜層が存在するためにクラックや剥離等が生じにくくなる。また、上部金属配線と接しているのはシリコン酸化膜なので絶縁特性は十分ある。このようにして信頼性の高い多層配線構造を持つ半導体装置が得られる。

実施例

以下、図面に基づいて本発明について更に詳しく説明する。

第１図から第４図は、本発明にかかる半導体装置の製造方法の一実施例の工程を示す部分拡大断面図である。

第１図において半導体基板１上に選択酸化法を用いてフィールド酸化膜２を形成した後、ゲート酸化膜３、ポリシリコンゲート４を順に形成し、イオン打ち込み法によりソース，ドレイン領域に拡散層５を設ける。次に、ボロンリンガラスなどの第１層間絶縁膜６を形成し、異方性エッチングによりコンタクトホール７を形成する。この上に１μ厚の第１アルミ配線８を形成し、第２層間絶縁膜９を約６０００Å形成する。第２層間絶縁膜９としては、プラズマＣＶＤ法で形成したシリコン酸化膜などが適している。次に有機シリコン含有液を約３０００Å塗布する。有機シリコン含有液としては $(C_6H_5)_nSi(OH)_{4-n}$ の構造を持つ化合物を含む溶液を用いる。有機シリコン含有液は細い溝部にも入り込むので、塗布前にあった基板上の凹凸はほとんどなくすことができる。次に半導体基板１に熱処理（室温から数段階に分けて温度を上げ、最終460℃で３０分）を施し有機シリコン薄膜１０を形成する（第２図）。この後半導体基板１を酸素プラズマ中に１０分間さらすと、有機シリコン薄膜１０の有機官能基が所定の深さまではずれ、シリコン酸化膜に変化する。よって、最初に形成した有機シリコン薄膜１０の膜厚が薄いところはほとんどシリコン酸化膜１１に変化し、膜厚が厚いところだけがシリコン酸化膜１１と有機シリコン薄膜１０の２層構造になる（第３図）。基板上に配線層間のスルーホール１２を設け、第２アルミ配線１３を形成する（第４図）。基板上に有機シリコン含有液を塗布して平坦化を施してあるため、第２アルミ配線１３は断線やショートが起こりにくくなっている。しかも第２アルミ配線１３と直接接しているのはシリコン酸化膜１１なので絶縁特性は十分ある。また、第１アルミ配線８と第２アルミ配線１３の層間膜の厚いところはシリコン酸化膜と有機シリコン薄膜の２層構造になっており、下層に有機シリコン薄膜層があるためクラックなどが入りにくい。

本発明による製造方法に用いる有機シリコン含有液は $RnSi(OH)_{4-n}$（Ｒ：アルキル基）の構造または $Si(OR)_4$（Ｒ：アルキル基）の構造を持った化合物を含むことが望ましく、中でも本実施例で用いた $(C_6H_5)_nSi(OH)_{4-n}$ を含む溶液が極めて優れた特性を示す。

発明の効果

本発明による製造方法を用いると、簡単な工程により配線金属層間の層間膜を平坦化することが

できる。しかもシリコン酸化膜と有機シリコン薄膜を組み合わせているため、絶縁性が高くクラックや剥離を生じにくく、信頼性の高い半導体装置を得ることができる。

本発明による製造方法は、液体の塗布で平坦化を行っているため、今後さらに素子の微細化が進んでも対応できる。このような製造方法は他にはなく、極めて産業上価値の高いものである。

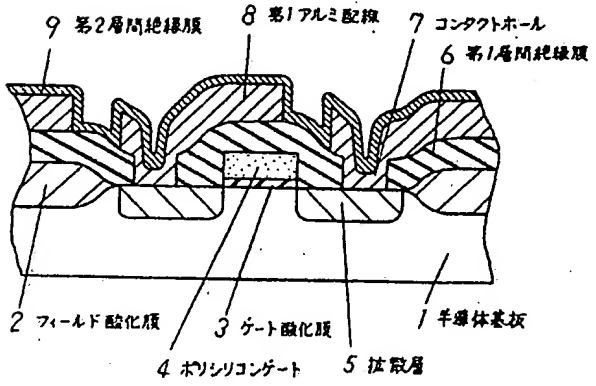
4、図面の簡単な説明

第1図から第4図は本発明により半導体装置を製造する場合の一実施例の工程を示し、第1図は本発明にかかる製造方法に用いる半導体基板の部分拡大断面図、第2図は有機シリコン薄膜形成後の半導体基板の部分拡大断面図、第3図は半導体基板を酸素プラズマにさらした後の半導体基板の部分拡大断面図、第4図は本発明にかかる製造方法を用いた後第2アルミ配線を形成した後の半導体基板の部分拡大断面図である。

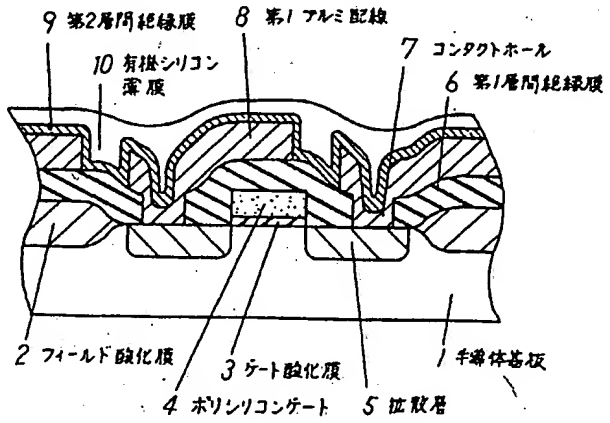
1……半導体基板、2……フィールド酸化膜、3……ゲート酸化膜、4……ポリシリコンゲート、5……拡散層、6……第1層間絶縁膜、7……コンタクトホール、8……第1アルミ配線、9……第2層間絶縁膜、10……有機シリコン薄膜、11……シリコン酸化膜、12……スルーホール、13……第2アルミ配線。

代理人の氏名　弁理士　中　尾　敏　男　ほか1名

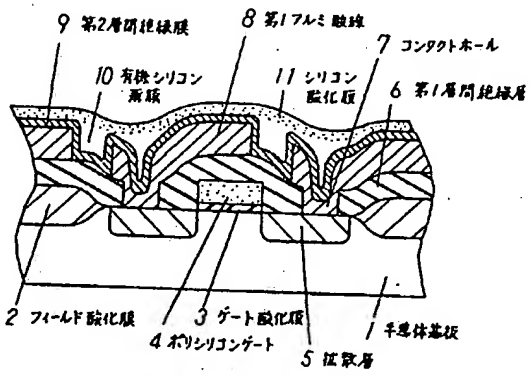
第　1　図



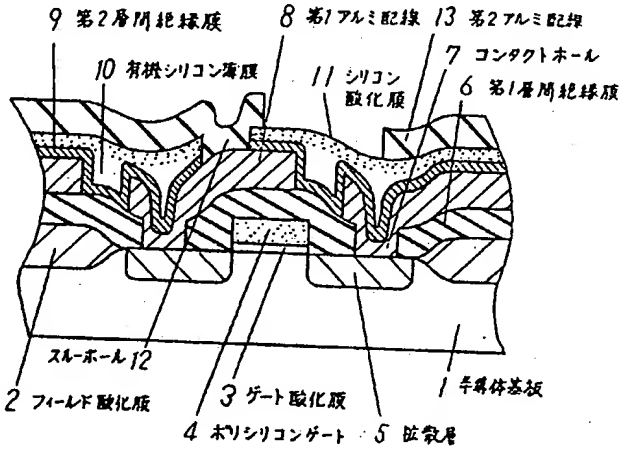
第　2　図



第 3 図


9 第2層間絶縁膜
8 第1アルミ配線
7 コンタクトホール
10 有機シリコン膜膜
11 シリコン酸化膜
6 第1層間絶縁膜
2 フィールド酸化膜
3 ゲート酸化膜
4 ポリシリコンゲート
5 拡散層
1 半導体基板

第 4 図


9 第2層間絶縁膜
8 第1アルミ配線
13 第2アルミ配線
10 有機シリコン膜膜
11 シリコン酸化膜
7 コンタクトホール
6 第1層間絶縁膜
スルーホール 12
2 フィールド酸化膜
3 ゲート酸化膜
4 ポリシリコンゲート
5 拡散層
1 半導体基板